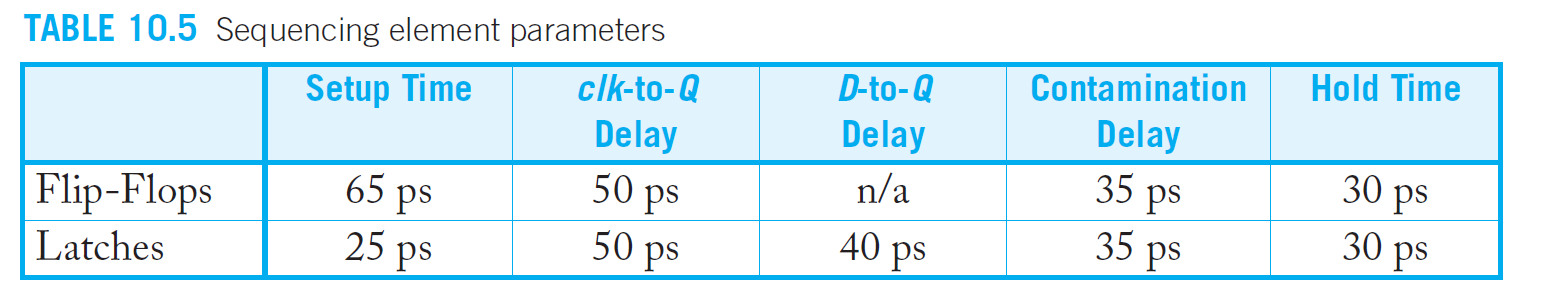
# ECE 4203

Homework 6

Solve problems 10.1-10.4 in Weste and Harris ***using Table 10.5***. They are repeated below for your convenience:



Problem 10.1)

For each of the following sequencing styles, determine the maximum logic propagation

delay available within a 500 ps clock cycle. Assume there is zero clock skew and

no time borrowing takes place.

a) Flip-flops

b) Two-phase transparent latches

c) Pulsed latches with 80 ps pulse widt

Problem 10.2)

Repeat Exercise 10.1 if the clock skew between any two elements can be up to 50 ps.

Problem 10.3)

For each of the following sequencing styles, determine the minimum logic contamination

delay in each clock cycle (or half-cycle, for two-phase latches). Assume there

is zero clock skew.

a) Flip-flops

b) Two-phase transparent latches with 50% duty cycle clocks

c) Two-phase transparent latches with 60 ps of nonoverlap between phases

d) Pulsed latches with 80 ps pulse width

Problem 4)

Repeat Exercise 10.3 if the clock skew between any two elements can be up to 50 ps.